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Products of
SJ company

(주) 에스제이컴퍼니
SJ company

Display Glass




1 Sodalime Glass, Gorilla Glass

Item	Specification
Glass Size	From 10mm × 10mm to over 370mm × 470mm
Glass Thickness	0.4 / 0.6 / 0.7 / 1.1 / 1.8 mm
Remark	Custom sizes are available to suit various manufacturing processes.

2 Non-Alkali Glass

Item	Specification
Glass Size	From 10mm × 10mm to over 370mm × 470mm
Glass Thickness	0.5 / 0.7mm
Remark	Custom sizes are available to suit various manufacturing processes.

3 Ultra Thin Glass

Item	Specification
Glass Size	round and square custom-size wafer
Glass Thickness	0.03mm ~
Surface Roughness	< 1nm RMS
Luminous transmittance TVD65(d=0.5mm)	91.7%

4 ITO Glass

Item	Specification
Glass Size	From 10mm × 10mm to over 370mm × 470mm
Glass Thickness	0.2 ~ 1.8mm
ITO Resistance	5 ~ 100Ω
ITO Thickness	200 ~ 4000Å
Transmitance	80 ~ 91%
Remark	Custom sizes are available to suit various manufacturing processes.

Deposition and Patterning Process

We offer ITO deposition on glass with thickness customized to customer requirements, including precision deposition and patterning of high-transparency, high-conductivity thin films on large-area glass.

- Metal : Cr, Cu , Ti, Au, Ag, Al, Ni, Mo, ITO etc
- Substrate : 2"~12" Wafer, 370x470mm, 1100x1300 Large Area

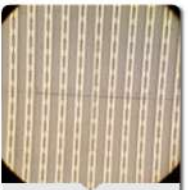
ITO/PDL
Patterned Glass

ITO/PDL
Patterned Glass

ITO
Patterned Glass

ITO/Ag/ITO
Patterned Glass

Au Patterned Glass

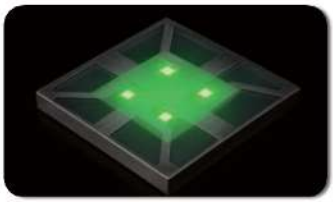


Ti/Cu
Patterned Glass

OLED TEST Substrate

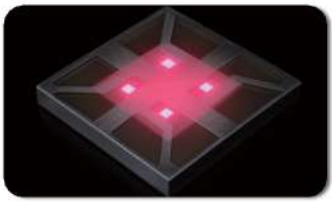
This substrate is designed for OLED material deposition and Encap processes, featuring precisely patterned anode and PDL structures on a glass base.

It is suitable for OLED emission TEG fabrication and utilizes deposition process technology optimized for the characteristics of OLED emissive materials.

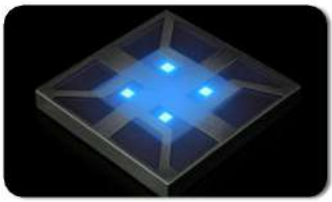


OLED TEST Substrate(Green)

Item	Specification
Glass Size	25X25mm ~ 370X470mm
Glass Thickness	0.5 / 0.7mm
Remark	Custom sizes are available to suit various manufacturing processes.



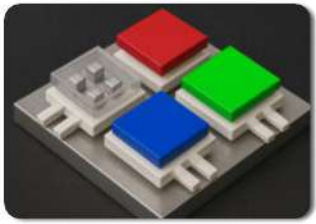
OLED TEST Substrate(Red)



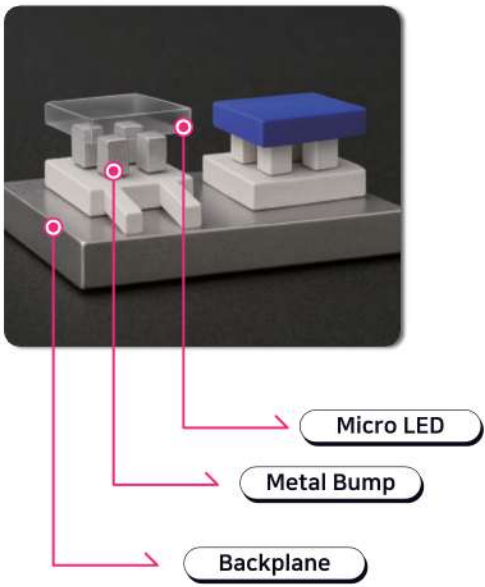
OLED TEST Substrate(Blue)

Deposition and Patterning for Micro LED

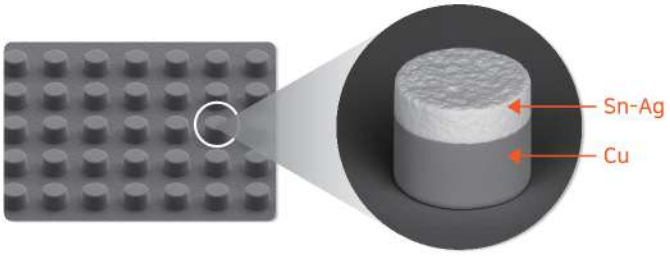
Deposition and Patterning for Micro

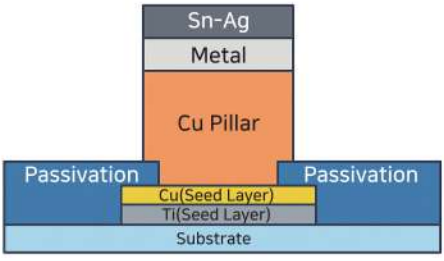


- Metal deposition for Micro LED transfer and bonding
- Precision deposition and patterning of metal layers (down to several micrometers) on large-area substrates
- Deposition process applicable to backplanes of various sizes, from small-scale to large-area formats



Cu /Sn-Ag Pillar Bump

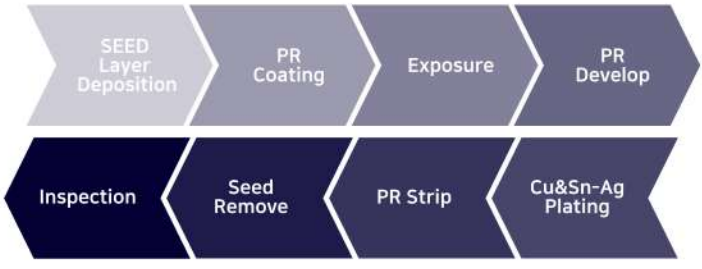




Cu (Copper) Pillar Bump technology is used in semiconductor packaging to connect chips and substrates.
The copper pillar-shaped bumps enable fine-pitch interconnections while ensuring high reliability.
This structure maintains the gap between the chip and substrate, providing excellent electrical performance and mechanical stability — making it a key advantage in advanced semiconductor packaging.

Substrate	Si Wafer , Glass Wafer
wafer size available	4 / 6 / 8 inch(*Custom size available)
Bump Material	Cu Pillar + Sn-ag Cap
Bump Diameter	≥20μm(Min)
Bump Pitch	≥40μm
Bump Height	≤70μm(Max) * Bump Dia와 1:1
Structure	Direct Cu Pillar+Sn-ag Cap
	Passivation + Cu Pillar+Sn-ag Cap
	Passivation + Cu Pillar+ Metal +Sn-ag Cap
Option Process	Metal:Ni / Cu
	Cap:Sn / Sn-ag / Au

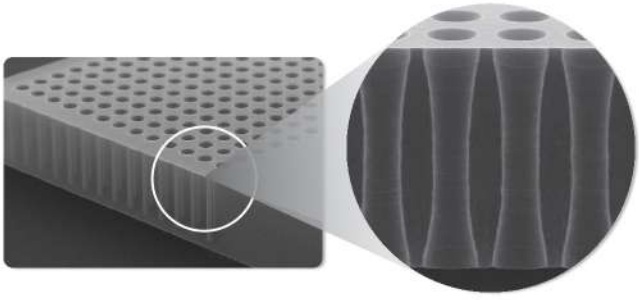
Cu/Sn-Ag Pillar Bump Process Flow



TGV(Through Glass Via)

Through-Glass Via (TGV) is a technology that creates vertical holes through glass substrates to enable electrical conduction, allowing the realization of high-performance and high-density circuits.

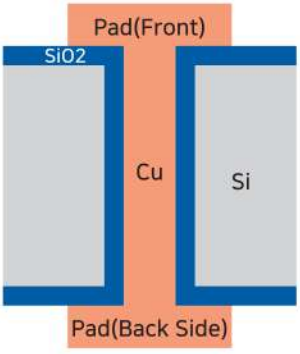
It is primarily used in next-generation semiconductor packaging as an interposer layer that electrically connects semiconductor chips and substrates.
The use of **Cu-filled vias** ensures excellent conductivity and reliability in advanced electronic applications.



Glass material	Borosilicate, Qz, etc
Substrate size available	4 / 6 / 8 inch & 510x515mm(*Custom size available)
Aspect ratio	10:1
Via Diameter	≥30μm(*Customizable)
Via Pitch	Via Dia x 2
Glass Thickness	≥300μm(*Customizable)

TSV(Through Silicon Via)

Through-Silicon Via (TSV) is a semiconductor packaging technology that forms vertical holes through a silicon wafer to interconnect chips.
This technique plays a critical role in enhancing chip performance and integration density.
It is widely used in high-performance semiconductors such as **High Bandwidth Memory (HBM)**, where fine-pitch, high-reliability interconnects are essential.



TSV Cross Section

wafer size available	4 / 6 / 8 inch
Via Diameter	≥20μm
Via Pitch	≥40μm
Si Thickness	≥300μm
Insulation(SiO2)	≤2μm(Thermal Oxidation)
Option Process	Pad(Metal:Cu / Ni /Au)
	RDL(Metal:Ti/Cu)